CHAPTER 9: MOS Diode Modeling

9.1 Diode IV Model

The diode IV modeling now supports a resistance-free diode model and a current-limiting feature by introducing a new model parameter *ijth* (defaulting to 0.1A). If *ijth* is explicitly specified to be zero, a resistance-free diode model will be triggered; otherwise two critical junction votages *Vjsm* for S/B diode and *Vjdm* for D/B diode will be computed from the value of *ijth*.

9.1.1 Modeling the S/B Diode

If the S/B saturation current I_{sbs} is larger than zero, the following equations is used to calculate the S/B diode current I_{bs}.

Case 1 - *ijth* is equal to zero: A resistance-free diode.

$$I_{bs} = I_{sbs}\left(\exp\left(\frac{V_{bs}}{NV_{tm}}\right) - 1\right) + G_{min}V_{bs}$$

(9.1)

where $NV_{tm} = NJ \cdot (KbT)/q$; *NJ* is a model parameter, known as the junction emission coefficient.

Case 2 - *ijth* is non-zero: Current limiting feature.

If $V_{bs} < Vjsm$

(9.2)

$$I_{bs} = I_{sbs}\left(\exp\left(\frac{V_{bs}}{NV_{tm}}\right) - 1\right) + G_{min}V_{bs}$$

otherwise

(9.3)

$$I_{bs} = ijth + \frac{ijth + I_{sbs}}{NV_{tm}}\left(V_{bs} - Vjsm\right) + G_{min}V_{bs}$$

with *Vjsm* computed by

$$Vjsm = NV_{tm}\ln\left(\frac{ijth}{I_{sbs}} + 1\right)$$

The saturation current I_{sbs} is given by

(9.4)

$$I_{sbs} = A_s J_s + P_s J_{ssw}$$

where J_s is the junction saturation current density, A_S is the source junction area, J_{ssw} is the sidewall junction saturation current density, P_s is the perimeter of the source junction. J_s and J_{ssw} are functions of temperature and can be written as

(9.5)

$$J_s = J_{s0}\exp\left(\frac{\dfrac{E_{g0}}{V_{tm0}} - \dfrac{E_g}{V_{tm}} + XTI\ln\left(\dfrac{T}{T_{nom}}\right)}{NJ}\right)$$

(9.6)

$$J_{ssw} = J_{s0sw} \exp\left(\dfrac{\dfrac{E_{g0}}{V_{tm0}} - \dfrac{E_g}{V_{tm}} + XTI\ln\left(\dfrac{T}{T_{nom}}\right)}{NJ}\right)$$

The energy band-gap E_{g0} and E_g at the nominal and operating temperatures are expressed by (9.7a) and (9.7b), repectively:

(9.7a)

$$E_{g0} = 1.16 - \dfrac{7.02 \times 10^{-4} T_{nom}^{\;2}}{T_{nom} + 1108}$$

(9.7b)

$$E_g = 1.16 - \dfrac{7.02 \times 10^{-4} T^{\,2}}{T + 1108}$$

In the above derivatoins, J_{s0} is the saturation current density at T_{nom}. If J_{s0} is not given, $J_{s0} = 1 \times 10^{-4}$ A/m^2. J_{s0sw} is the sidewall saturation current density at T_{nom}, with a default value of zero.

If I_{sbs} is not positive, I_{bs} is calculated by

(9.8)

$$I_{bs} = G_{min} \cdot V_{bs}$$

9.1.2 Modeling the D/B Diode

If the D/B saturation current I_{sbd} is larger than zero, the following equations is used to calculate the D/B diode current I_{bd}.

Case 1 - *ijth* is equal to zero: A resistance-free diode.

(9.9)

$$I_{bd} = I_{sbd}\left(\exp\left(\frac{V_{bd}}{NV_{tm}}\right) - 1\right) + G_{\min}V_{bd}$$

Case 2 - *ijth* is non-zero: Current limiting feature.

If $V_{bd} < Vjdm$

(9.10)

$$I_{bd} = I_{sbd}\left(\exp\left(\frac{V_{bd}}{NV_{tm}}\right) - 1\right) + G_{\min}V_{bd}$$

otherwise

(9.11)

$$I_{bd} = ijth + \frac{ijth + I_{sbd}}{NV_{tm}}\left(V_{bd} - Vjdm\right) + G_{\min}V_{bd}$$

with *Vjdm* computed by

$$Vjdm = NV_{tm} \ln\left(\frac{ijth}{I_{sbd}} + 1\right)$$

The saturation current I_{sbd} is given by

(9.12)

$$I_{sbd} = A_d J_s + P_d J_{ssw}$$

where A_d is the drain junction area and P_d is the perimeter of the drain junction. If I_{sbd} is not positive, I_{bd} is calculated by

(9.13)

$$I_{bd} = G_{\min} \cdot V_{bd}$$

9.1.3 Model Parameter Lists

The diode DC model parameters are listed in Table 9-1.

Symbols used in equation	Symbols used in SPICE	Description	Default	Unit
Js0	js	Saturation current density	1e-4	A/m^2
Js0sw	jssw	Side wall saturation current density	0	A/m
NJ	nj	Emission coefficient	1	none
XTI	xti	Junction current temperature exponent coefficient	3.0	none
ijth	ijth	Limiting current	0.1	A

Table 9-1.   MOS diode model parameters.

9.2 MOS Diode Capacitance Model

Source and drain junction capacitance can be divided into two components: the junction bottom area capacitance C_{jb} and the junction periphery capacitance C_{jp}. The formula for both the capacitances is similar, but with different model parameters. The equation of C_{jb} includes the parameters such as C_j, M_j, and P_b. The equation of C_{jp} includes the parameters such as C_{jsw}, M_{jsw}, P_{bsw}, C_{jswg}, M_{jswg}, and P_{bswg}.

9.2.1 S/B Junction Capacitance

The S/B junction capacitance can be calculated by

If $P_s > W_{eff}$

$$Capbs = A_s C_{jbs} + \left(P_s - W_{eff}\right) C_{jbssw} + W_{eff} C_{jbsswg}$$

(9.14)

Otherwise

(9.15)

$$Capbs = A_s C_{jbs} + P_s C_{jbsswg}$$

where C_{jbs} is the unit bottom area capacitance of the S/B junction, C_{jbssw} is the periphery capacitance of the S/B junction along the field oxide side, and C_{jbsswg} is the periphery capacitance of the S/B junction along the gate oxide side.

If C_j is larger than zero, C_{jbs} is calculated by

if $V_{bs} < 0$

(9.16)

$$C_{jbs} = C_j \left(1 - \frac{V_{bs}}{P_b} \right)^{-M_j}$$

otherwise

(9.17)

$$C_{jbs} = C_j \left(1 + M_j \frac{V_{bs}}{P_b} \right)$$

If C_{jsw} is large than zero, C_{jbssw} is calculated by

if $V_{bs} < 0$

(9.18)

$$C_{jbssw} = C_{jsw} \left(1 - \frac{V_{bs}}{P_{bsw}} \right)^{-M_{jsw}}$$

otherwise

(9.19)

$$C_{jbssw} = C_{jsw} \left(1 + M_{jsw} \frac{V_{bs}}{P_{bsw}} \right)$$

If C_{jswg} is larger than zero, C_{jbsswg} is calculated by

if $V_{bs} < 0$

(9.20)

$$C_{jbsswg} = C_{jswg} \left(1 - \frac{V_{bs}}{P_{bswg}} \right)^{-M_{jswg}}$$

otherwise

(9.21)

$$C_{jbsswg} = C_{jswg} \left(1 + M_{jswg} \frac{V_{bs}}{P_{bswg}} \right)$$

9.2.2 D/B Junction Capacitance

The D/B junction capacitance can be calculated by

If $P_d > W_{eff}$

(9.22)

$$Capbd = A_d C_{jbd} + (P_d - W_{eff}) C_{jbdsw} + W_{eff} C_{jbdswg}$$

Otherwise

(9.23)

$$Capbd = A_d C_{jbd} + P_d C_{jbdswg}$$

where C_{jbd} is the unit bottom area capacitance of the D/B junction, C_{jbdsw} is the periphery capacitance of the D/B junction along the field oxide side, and C_{jbdswg} is the periphery capacitance of the D/B junction along the gate oxide side.

If C_j is larger than zero, C_{jbd} is calculated by

if $V_{bd} < 0$

(9.24)

$$C_{jbd} = C_j \left(1 - \frac{V_{bd}}{P_b} \right)^{-M_j}$$

otherwise

(9.25)

$$C_{jbd} = C_j \left(1 + M_j \frac{V_{bd}}{P_b} \right)$$

If C_{jsw} is large than zero, C_{jbdsw} is calculated by

if $V_{bd} < 0$

$$(9.26)$$

$$C_{jbdsw} = C_{jsw} \left(1 - \frac{V_{bd}}{P_{bsw}} \right)^{-M_{jsw}}$$

otherwise

$$(9.27)$$

$$C_{jbdsw} = C_{jsw} \left(1 + M_{jsw} \frac{V_{bd}}{P_{bsw}} \right)$$

If C_{jswg} is larger than zero, C_{jbdswg} is calculated by

if $V_{bd} < 0$

$$(9.28)$$

$$C_{jbdswg} = C_{jswg} \left(1 - \frac{V_{bd}}{P_{bswg}} \right)^{-M_{jswg}}$$

otherwise

$$(9.29)$$

$$C_{jbdswg} = C_{jswg} \left(1 + M_{jswg} \frac{V_{bd}}{P_{bswg}} \right)$$

9.2.3 Temperature Dependence of Junction Capacitance

The temperature dependence of the junction capacitance is modeled. Both zero-bias unit-area junction capacitance (C_j, C_{jsw} and C_{jswg}) and built-in potential of the junction (P_b, P_{bsw} and P_{bswg}) are temperature dependent and modeled in the following.

For zero-bias junction capacitance:

$$(9.30a)$$

$$C_j(T) = C_j(T_{nom}) \cdot (1 + tcj \cdot \Delta T)$$

$$(9.30b)$$

$$C_{jsw}(T) = C_{jsw}(T_{nom}) \cdot (1 + tcjsw \cdot \Delta T)$$

$$(9.30c)$$

$$C_{jswg}(T) = C_{jswg}(T_{nom}) \cdot (1 + tcjswg \cdot \Delta T)$$

For the built-in potential:

$$(9.31a)$$

$$P_b(T) = P_b(T_{nom}) - tpb \cdot \Delta T$$

$$(9.31b)$$

$$P_{bsw}(T) = P_{bsw}(T_{nom}) - tpbsw \cdot \Delta T$$

$$(9.31c)$$

$$P_{bswg}(T) = P_{bswg}(T_{nom}) - tpbswg \cdot \Delta T$$

In Eqs. (9.30) and (9.31), the temperature difference is defined as

$$(9.32)$$

$$\Delta T = T - T_{nom}$$

The six new model parameters in the above equations are described in Table 9-2.

9.2.4 Junction Capacitance Parameters

The following table give a full description of those model parameters used in the diode junction capacitance modeling.

Symbols used in equation	Symbols used in SPICE	Description	Default	Unit
Cj	cj	Bottom junction capacitance per unit area at zero bias	5e-4	F/m^2
Mj	mj	Bottom junction capacitance grading coefficient	0.5	none
Pb	pb	Bottom junction built-in potential	1.0	V
Cjsw	cjsw	Source/drain sidewall junction capacitance per unit length at zero bias	5e-10	F/m
Mjsw	mjsw	Source/drain sidewall junction capacitance grading coefficient	0.33	none
Pbsw	pbsw	Source/drain side wall junction built-in potential	1.0	V
Cjswg	cjswg	Source/drain gate side wall junction capacitance per unit length at zero bias	Cjsw	F/m
Mjswg	mjswg	Source/drain gate side wall junction capacitance grading coefficient	Mjsw	none
Pbswg	pbswg	Source/drain gate side wall junction built-in potential	Pbsw	V
tpb	tpb	Temperature coefficient of Pb	0.0	V/K
tpbsw	tpbsw	Temperature coefficient of Pbsw	0.0	V/K

Symbols used in equation	Symbols used in SPICE	Description	Default	Unit
tpbswg	tpbswg	Temperature coefficient of Pbswg	0.0	V/K
tcj	tcj	Temperature coefficient of Cj	0.0	1/K
tcjsw	tcjsw	Temperature coefficient of Cjsw	0.0	1/K
tcjswg	tcjswg	Temperature coefficient of Cjswg	0.0	1/K

Table 9-2. MOS Junction Capacitance Model Parameters.